REMARKS

Claims 1-7, 9-17, 20-34, 36-38, 41-43, 45 and 46 are pending in the present application. All claims were rejected in the Office Action dated July 25, 2006. Reconsideration of all rejected claims is requested in light of the amendments and arguments presented below.

Claim Rejections under 35 U.S.C. §112

Claims 20 and 30 are rejected under 35 USC 112, first paragraph, as failing to comply with the enablement requirement. Claim 20 was rejected because claim 20 recites a memory system is a SmartMedia card and this was considered to lack enablement because the memory system comprised a controller (per claim 6 from which claim 20 depends). Claim 20 is amended to delete the element "a SmartMedia card." Therefore, it is believed that the rejection is overcome.

Claim 30 was rejected as failing to comply with the enablement requirement because claim 29 (from which claim 30 depends) recited, "the memory system is a memory card" and claim 21 (from which claim 29 depends) recites "a memory system on a first chip." Claim 29 is amended to recite, "the memory system is in a memory card." Therefore, it is believed that the rejection is overcome.

Claim Rejections under 35 U.S.C. §102

Claims 6-7, 9-14, 16-17, 34, 36-38, and 41-43 are rejected under 35 USC 102(e) as being anticipated by Moshayedi, USP 2002/0091965.

Claim 6 recites, "a first storage element on the first chip, the first storage element containing a first counter and a first threshold" and "a second storage element on the second chip, the second storage element containing a second counter and a second threshold." No such first and second storage elements on first and second chips appear to be disclosed by Moshayedi. In particular, the cited portions of Moshayedi (paragraphs [0050] and [0053]) appear to describe process 400 (process "for the early detection of impending failure," paragraph [0047]). However, locations where a counter and threshold

are stored do not appear to be disclosed. Process 400 (see Figure 4) includes "receive updated spares count" 420. However, Moshayedi does not appear to indicate where the spares count is received from. Thus, these claim elements have not been shown.

Claim 6 recites, "the controller reassigns a spare unit of erase in response to a request from the host system." The Office Action cited paragraphs [0032]-[0037] as showing these claim elements. However, no such reassignment in response to a request from the host system appears to be shown. In particular, paragraphs [0032]-[0037] appear to disclose communication between a host and a memory system, but no request to a controller or a reassignment in response to such a request appears to be shown. Therefore, claim 6 is submitted to be allowable.

Claims 7, 9-17 and 20 depend from claim 6 and are therefore submitted to be allowable at least for depending from an allowable base claim.

Claim 34 is amended to replace "means for decrementing the counter" by "a counter" and to delete "means for storing a counter," and add "means for storing the counter" after "a counter" so that proper antecedent basis is provided. The counter of claim 34 is not a means-plus-function limitation. Therefore, MPEP 2184(II)(A) is not believed to apply to this limitation.

Moshayedi does not appear to disclose "a counter being decremented." The Office Action appears to take the position that Moshayedi's disclosure of "a counter that is incremented" (claim 36) discloses a counter that is either incremented or decremented and cites a dictionary definition to support this position. However, it is submitted that to interpret "incremented" to include "decremented" is contrary to the ordinary meaning of the terms. It is further submitted that one of ordinary skill in the art would not understand Moshayedi to disclose decrementing a counter. In particular, it appears that the only reference in Moshayedi to updating a counter each time a new spare location is used describes "a counter that is incremented each time," claim 36.

With respect to the dictionary definition, it appears that the cited definition, "the amount of positive or negative change in the value of one or more of a set of variables." refers to the noun "increment." This would not indicate that the counter "that is incremented" of Moshayedi is decremented. Furthermore, to the extent that the Office Action takes the term "incremented" of Moshayedi as a generic term covering both

incrementing and decrementing, the use of this term would not specifically indicate that the counter is decremented. Because Moshayedi does not disclose a counter being decremented, claim 34 is submitted to be allowable.

Claims 36-38 depend from claim 34 and are therefore submitted to be allowable at least for depending from an allowable base claim.

Claim 41 recites, "saving the indication." The Office Action indicated that paragraph [0056] showed saving an indication. Paragraph [0056] discloses "information is updated and stored." However, it is not disclosed that such information includes an indication "arranged to indicate that the non-volatile system is nearing the condition which renders the non-volatile memory system as being substantially unreliable" of claim 41. Because saving of such an indication has not been identified in Moshayedi, anticipation has not been shown.

Claims 42-43 depend from claim 41 and are therefore submitted to be allowable at least for depending from an allowable base claim.

Claim Rejections under 35 U.S.C. §103

Claims 1-5 and 15 are rejected under 35 USC 103(a) as being unpatentable over Moshayedi in view of Auclair et al., US 6,016,530. The Office Action acknowledged that Moshayedi fails to teach using error correction codes. Auclair was cited as teaching using error correction code. However, the motivation to combine the teaching of Auclair with Moshayedi is not understood. In particular, the portion of Auclair cited as providing this motivation (column 1, lines 34-60) does not appear to discuss error correction codes. The cited text appears to discuss differences between hard disk drives and solid-state memory systems and mentions some advantages of solid-state memory systems, including lower power. Because the cited text does not discuss error correction code, it is not seen how it could provide motivation to modify Moshayedi by adding error correction code features. It was also asserted in the office action that including ECC for fault tolerance is well known. However, no reference was cited to support this assertion and the assertion is traversed. MPEP 2143.01 states, "The prior art must suggest the desirability of the claimed invention." The claimed invention of claim 1 includes "calculating error correction code data" and "updating a counter each time a spare unit of erase of the

plurality of spare units of erase is reassigned." Thus, the prior art must suggest the desirability of such a combination. Because no such motivation has been shown, no *prima facie* case of obviousness has been made with respect to claim 1.

Claims 2-5 depend from claim 1 and are submitted to be allowable at least for depending from an allowable base claim. In addition, claims 2-5 recite additional claim limitations that further distinguish over the cited references.

For example, claim 2 recites "decrementing the counter." As discussed above, the cited reference (Moshayedi) does not appear to show this feature.

Claim 15 recites, "an individual one of the first plurality of spare units of erase is a sector." The Office Action acknowledged that Moshayedi fails disclose these features, but cited Auclair as disclosing these features. However, no adequate motivation was provided for combining the teachings of Moshayedi and Auclair to obtain the invention of claim 15. In particular, the Office action cited column, lines 34-60 of Auclair as disclosing certain advantages. However, the cited text appears to refer to advantages of solid-state memory systems over hard disk drives, not advantages of having a spare unit of erase that is a sector. The Office Action also indicated that it was "well-known in the art to allocate flash memory sections as sectors," page 14, line 7. No reference was cited to support this assertion and the assertion is traversed. Furthermore, even if such allocation (assumed to refer to allocation of a unit of erase) is considered well known, a motivation to combine such allocation with the teaching of Moshayedi is not provided. "The prior art must suggest the desirability of the claimed invention," MPEP 2143.01(I) (emphasis added). Because no adequate motivation to combine the references has been provided, no *prima facie* case of obviousness has been stated with respect to claim 15.

Claims 20, 45, and 46 were rejected under 35 USC 103(a) as being unpatentable over Moshayedi in view of Official Notice. The Office Action acknowledged that Moshayedi fails to teach the memory card formats recited in these claims. The Examiner took Official Notice that "one of ordinary skill in the art would have thought it obvious to have implemented any of one of the above-mentioned types of memory cards in the invention of Moshayedi," page 14, lines 13-15. However, MPEP 2144.03A. states, "Official notice unsupported by documentary evidence should only be taken by the

examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known." It is submitted that, what one of ordinary skill in the art would have thought obvious is not a fact capable of instant and unquestionable demonstration. Therefore, taking notice of what one of skill would have thought is inappropriate and is simply an assertion that the claimed invention is obvious as a matter of fact, without providing any rationale. It was further asserted that the recited cards are well known. However, even if such cards were well known, this still does not provide a motivation to combine such cards with the teachings of Moshayedi. Without such motivation, no *prima facie* case of obviousness is stated with respect to these claims. Therefore, claims 20, 45 and 46 are submitted to be allowable.

Claims 21-31 were rejected under 35 USC 103(a) as being unpatentable over Moshayedi in view of Kozakai et al., US 6,643,725. Claim 21 recites, "a memory system on a first chip" and "a controller on the first chip." The Office Action acknowledged that these features were not shown by Moshayedi, but cited Kozakai as showing these features. One cited motivation to combine the references was "because the invention of Kozakai et al. conserves and utilizes space efficiently in a memory system (column 1 lines 45-55 and column 2 line 65 through column 3 line 2)," Office Action, page 18, lines 3-5. However, the cited portions of text do not appear to refer to such advantages of placing a memory system and controller on a single chip. It appears that the cited portion refers to advantages of a memory system that does not have a separate program memory for testing or debugging programs. "It is an object of the invention to provide a memory card in which a data processor incorporated therein can be caused to execute new programs for purposes including testing or debugging without adding a separate program memory." Column 1, lines 51-54. Thus, the absence of the program memory appears to be the advantage, not integration of a memory system and controller on one chip. Another cited motivation was that "a single-chip memory system operates faster and consumes less power than a multi-chip configuration (column 12 lines 43-46)," Office Action, page 18, lines 5-6. The cited text refers to advantages over multi-chip configurations. However, this appears to be in reference to an arrangement having a separate program

memory. "Since a buffer memory used for writing and reading file data can be also used as a program memory, separate programs for purposes such as testing or debugging can be executed using the buffer memory without any additional program memory." Column 12, lines 50-54. Thus, no motivation is provided for combining the single chip arrangement of Kozakai with the teaching of Moshayedi.

Claims 22-31 depend from claim 21 and are therefore submitted to be allowable at least for depending from an allowable base claim. In addition, claims 22-31 recite additional limitations that further distinguish over the cited references.

Claim 28 recites, "an individual one of the plurality of units of erase is a sector, and an individual one of the plurality of spare units of erase is a spare sector." The Office Action cited Moshayedi, Figure 2, paragraph [0039], which appears to show a row or location having four sectors. The Office Action also cited Kozakai (column 5, lines 6-18). However, the cited portion of Kozakai does not appear to disclose the unit of erase used and it is not clear how the "location" of Moshayedi is related to the cited text of Kozakai. Because neither Moshayedi nor Kozakai discloses that a unit of erase is a sector, claim 28 is further distinguished over the cited combination.

Claims 32 and 33 were rejected under 35 USC 103(a) as being unpatentable over Moshayedi in view of Kozakai et al., further in view of Shaberman et al., US 5,761,732. Claim 32 recites, "the information is one of, audio information, and wireless information." Claim 31, from which claim 32 depends recites, "the host is arranged to capture information and to attempt to store the information in the memory system." The Office Action acknowledged that Moshayedi and Kozakai fail to teach information being one of audio information and wireless information, but cited Shaberman as showing these claim features. However, no adequate motivation appears to be provided for combining the teaching of Shaberman with the other references to obtain the claimed inventions of claims 32 and 33. The Office Action stated, "This [combination] would have been obvious because the invention of Shaberman et al. allows for interchangeability of memory cards in differing systems (column 2 lines 11-16)," page 21, lines 1-3. However, it is not seen how modifying the teachings of Moshayedi and Kozakai according to the teaching of Shaberman would allow for interchangeability of cards. In particular, the

modification would involve storing audio or wireless information and it is not seen how storing such information would increase interchangeability. Because no adequate motivation to combine the references has been provided, no *prima facie* case of obviousness is made with respect to claims 32 and 33.

CONCLUSION

In view of the amendments and remarks contained herein, it is believed that all claims are in condition for allowance and an indication of their allowance is requested. However, if the Examiner is aware of any additional matters that should be discussed, a call to the undersigned attorney at: (415) 318-1160 would be appreciated.

Respectfully submitted,

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Date